AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the above-referenced application.

Listing of Claims:

1. (Currently Amended) A method of accessing data memory, comprising:

writing data to a first memory location and to a second memory location in response to a request to write data to a memory address that corresponds to both locations, wherein the first and second memory locations are mirrored;

in response to a request to read data from the memory address, reading data from the first memory location or the second memory location based on load balancing; ~~and~~

running tests to determine if one of the first memory location and the second memory location has failed;

in response to failure of one of the first and second memory locations, transitioning into a failover state and causing a non-failed one of the first memory location and the second memory location to be a primary memory location; and

accessing data from the ~~second~~ primary memory location in response to a request while in the failover state to access data at the memory address ~~when memory hardware corresponding to the first memory location has failed~~.

2. (Original) A method, according to claim 1, wherein accessing the data memory includes requesting access to a specific one of the first and second memory locations.

3. (Original) A method, according to claim 1, wherein the memory address contains a portion that is common to both the first memory location and the second memory location.

4. (Original) A method, according to claim 1, wherein hardware coupled to the memory causes data written using the memory address to be automatically written to the first memory location and the second memory location.

5. (Currently amended) A method, according to claim 1, wherein software causes the data ~~written using the memory address to be~~ written to the first memory location and the second memory location to be written using a first set of commands that writes the data to the first memory location and a second set of commands that writes the data to the second memory location.

6. (Original) A method, according to claim 1, wherein load balancing includes toggling at least one variable between a first state and a second state and wherein data is read from the first location when the at least one variable is in the first state and from the second location when the at least one variable is in the second state.

7. (Original) A method, according to claim 1, further comprising:

coupling a director board to the memory; and

coupling one of: a host, a disk, and a communications link to the director board.

8. (Original) A method, according to claim 7, further comprising:

transferring data between the memory and the director board.

9. (Original) A method, according to claim 7, further comprising:

the director board causing data to be transferred between the memory and one of: the host, the disk, and the communication link.

10. (Currently Amended) Computer software, stored in a computer-readable medium, that accesses data memory, comprising:

machine executable code that writes data to a first memory location and to a second memory location in response to a request to write data to a memory address that corresponds to both locations, wherein the first and second memory locations are mirrored;

machine executable code that reads data from the first memory location or the second memory location based on load balancing in response to a request to read data from the memory address; ~~and~~

machine executable code that runs tests to determine if one of the first memory location and the second memory location has failed;

machine executable code that transitions into a failover state and causes a non-failed one of the first memory location and the second memory location to be a primary memory location in response to failure of one of the first and second memory locations; and

machine executable code that accesses data from the ~~second~~ primary memory location in response to a request while in the failover state to access data at the memory address ~~when memory hardware corresponding to the first memory location has failed~~.

11. (Previously presented) The computer software stored in a computer readable medium according to claim 10, further comprising:

machine executable code that services requests to access to a specific one of the first and second memory locations.

12. (Previously presented) The computer software stored in a computer readable medium according to claim 10, wherein the memory address contains a portion that is common to both the first memory location and the second memory location.

13. (Currently amended) The computer software stored in a computer readable medium according to claim 10, further comprising:

machine executable code that causes the data ~~written using the memory address to be~~ written to the first memory location and the second memory location to be written using a first set of commands that writes the data to the first memory location and a second set of commands that writes the data to the second memory location.

14. (Previously presented) The computer software stored in a computer readable medium according to claim 10, further comprising:

machine executable code that toggles at least one variable between a first state and a second state wherein data is read from the first location when the at least one variable is in the first state and from the second location when the at least one variable is in the second state.

15. (Currently Amended) A data storage device, comprising:

a plurality of disk drives;

an internal volatile memory; and

a plurality of directors coupled to the memory, wherein some of the directors are coupled to the disk drives and some of the directors allow external access to the data storage device and wherein each of the directors access the memory by writing data to a first memory location and to a second memory location in response to a request to write data to a memory address that corresponds to both locations, wherein the first and second memory locations are mirrored, in response to a request to read data from the memory address, the directors read data from the first memory location or the second memory location based on load balancing, the directors run tests to determine if one of the first memory location and the second memory location has failed, the directors transition into a failover state and cause a non-failed one of the first memory location and the second memory location to be a primary memory location in response to failure of one of the first and second memory locations, and the directors access data from the ~~second~~ primary memory location in response to a request while in the failover state to access data at the memory address ~~when memory hardware corresponding to the first memory location has failed~~.

16. (Original) A data storage device, according to claim 15, wherein the directors request access to a specific one of the first and second memory locations.

17. (Original) A data storage device, according to claim 15, wherein the memory address contains a portion that is common to both the first memory location and the second memory location.

18. (Original) A data storage device, according to claim 15, wherein hardware coupled to the memory causes data written using the memory address to be automatically written to the first memory location and the second memory location.

19. (Currently amended) A data storage device, according to claim 15, wherein software causes the data ~~written using the memory address to be~~ written to the first memory location and the second memory location to be written using a first set of commands that writes the data to the first memory location and a second set of commands that writes the data to the second memory location.

20. (Original) A data storage device, according to claim 15, wherein load balancing includes toggling at least one variable between a first state and a second state and wherein data is read from the first location when the at least one variable is in the first state and from the second location when the at least one variable is in the second state.